1 MHz 8-Channel 12- or 16-Bit Analog Input Card and MEGA-FIFO 128 Million Sample Buffer

CIO-DAS16-M1, 1 MHz A/D card shown smalelr than actual size.

CIO-DAS16-M1 Series

3 YEAR WARRANTY

- **Blazing Fast Analog Input of 1 MHz Continuous to MEGA-FIFO with Sample Size Limited Only by the Size of Memory on the MEGA-FIFO Board**
- **Pre-Trigger and Post-Trigger Buffers of Unlimited Size**
- **Programmable 256-Step Channel/Gain Queue (12-Bit Version Only)**
- **DT-CONNECT Interface for High Speed Direct Transfer of Analog Data to MEGA-FIFO, Array Processors and Other Accessories**
- **32 Digital I/O Lines (82C55)**
- **LabVIEW Drivers Available**

The CIO-DAS16/M1, when combined with a MEGA-FIFO, can acquire sample sets of up to 128 million samples at full speed.

The CIO-DAS16-M1 employs the DT-Connect and MEGA-FIFO sample buffer board to acquire huge sample sets, completely independent of PC bus rates or other simultaneous processes.

High speeds are also possible and large sample sets can be processed directly to PC bus and PC memory because the CIO-DAS16/M1 uses a FIFO buffer and the REP-INSW command to transfer blocks at high speed into PC memory.

Connector Compatible

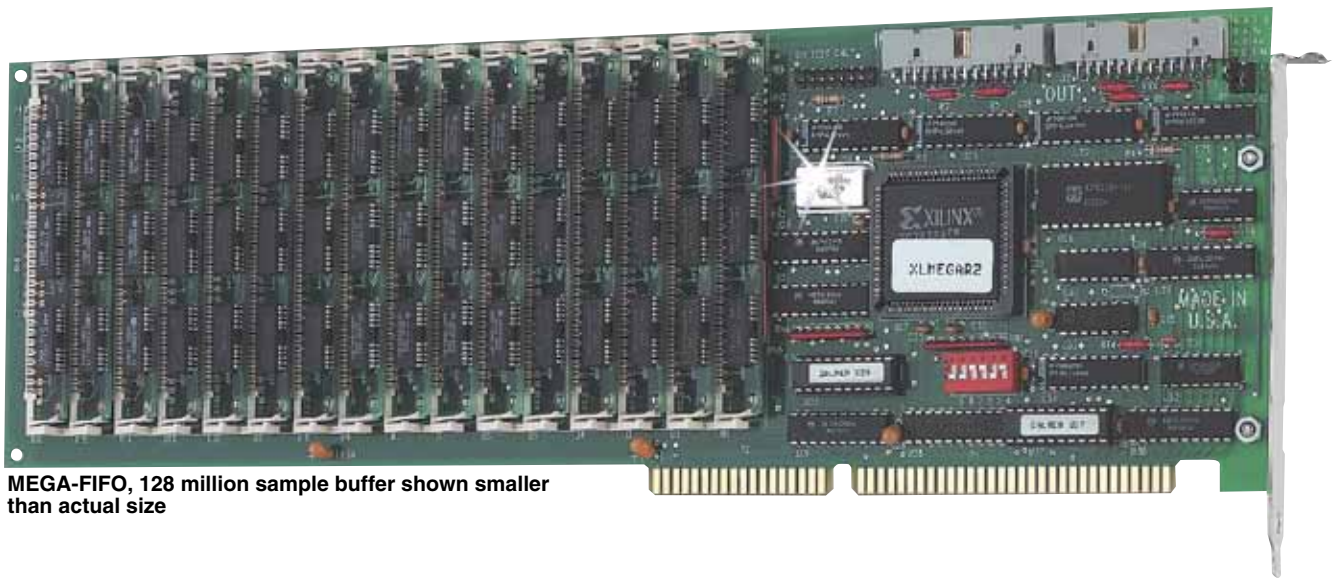
The CIO-DAS16/M1 is connector compatible with the older, original DAS-16. The control registers are very similar to the CIO-DAS16/330i, so adapting low-level drivers to the CIO-DAS16/M1 is a snap. Use the Universal Driver language driver software, and programs written for the CIO-DAS16/M1 will run other DAS-16 family boards as well.

Streaming Software

Streaming high speed samples to memory, RAM disk or hard disk is easy with the CIO-DAS16/M1's advanced architecture. The Universal Library includes modes for streaming data to files under program control.

Analog Inputs

The analog input section of the CIO-DAS16/M1 has been designed for high speed, flexibility and accuracy in a number of configurations and ranges. The analog signals are brought on board by a standard 37-pin D connector directly to balanced multiplexors. The multiplexors are configured as eight channels of differential input. Differential inputs can reject noise and ground loops (common mode voltages).



MEGA-FIFO, 128 million sample buffer shown smaller than actual size

Signals are amplified by a programmable gain amplifier prior to conversion by the A/D converter.

An integral sample and hold captures the signal, which is then converted by the A/D converter. The 12-bit A/D converter provides a resolution of 1 in 4095 parts of full scale.

The speed of data gathering may vary from less than 1 Hz to 1 MHz. Maximum acquisition speed is dependent on the method of triggering and data transfer.

REP INSW Transfer

REP INSW (Repeat Input String) is a 286/386/486/pentium class CPU instruction which allows the PC to transfer large amounts of data using one instruction. The data is transferred at the maximum rate allowed by the bus. On a typical 286 AT, this rate is 2 Mbyte/sec or 1 sample every microsecond.

In order to employ REP INSW, the A/D board must have a FIFO buffer to accumulate sample data. The CIO-DAS16/M1 has a 1024 sample buffer. When it is half full (512 samples), an interrupt generated by the DAS16/M1 starts an interrupt service routine which executes the instruction REP INSW, which transfers the data to PC memory and empties the FIFO buffer. The data is transferred completely to the background and no unreasonable demands are placed on the PC's resources. For example, screen updates need not be suspended!

Gain and Range Programming

No need to set switches to select an analog input range: the analog input range is fully programmable. A programmable gain queue controls both the unipolar/bipolar setting and the amplification of the analog input signal (on 12-bit board only).

METHOD	MAX A/D Speed
DT-Connect to MEGA-FIFO	1MHz
REP INSW to PC Memory	330KHz
Polled by software	4KHz-20KHz
Interrupt Service Routine	(no REP INSW) 4KHz - 20KHz

Gain Queue Programming

The channel/gain queue may be loaded with a sequence of between 1 and 256 channel+gain (CGQ) codes. When an analog input run is started, data will be acquired from the channels in the order specified by the CGQ. The programmable gain amplifier will be switched to the appropriate gain for the channel selected.

After the CGQ is loaded with a sequence of up to 256 different channel/gain combinations, all A/D channel and gain control are derived from the CGQ. The CGQ is automatically restarted when the last CGQ entry written is reached. For example, if you load 5 CGQ steps into the CGQ, the 1st, 6th, 11th, etc., A/D sample in a run is controlled by the 1st entry in the CGQ. In this manner, large sample runs can be precisely controlled.

MEGA-FIFO Data Acquisition Buffer

The MEGA-FIFO allows you to acquire up to 128 million samples of A/D data without using any CPU or bus time. Because the MEGA-FIFO employs the DT-Connect board-to-board link, the PC bus is bypassed entirely. Supporting both DT-Connect in and out, the MEGA-FIFO may be used to hold sampled data or to update an output board.

CIO-DAS16-M1, 1 MHz A/D card shown smaller than actual size

Windows and high performance accessories pose significant resource challenges to fast A/D applications. Taken one at a time, disk controllers, LAN interfaces, mega-pixel display boards and fast A/D boards operate well within bus specifications, but, when combined into a system, will exceed bus bandwidth. To acquire large sample sets at high speed, the data acquisition system must bypass the PC bus.

The MEGA-FIFO memory uses Single Inline Memory Modules just like those on your CPU board. They are available from many sources and the price of SIMM's continues to decline. The MEGA-FIFO will accept (30-pin x 9) 256 K, 1 MB, 4 MB and the newest 16 MB SIMM's. It does not come with any memory, which must be user-supplied.

The MEGA-FIFO can transfer through either the DT-Connect or the PC bus. The DT-Connect maximum rate is 1 million samples per second. The PC bus maximum rate is 900 K samples per second. Data may be transferred into or out of the MEGA-FIFO via the DT-Connect or the PC bus, but not through both at the same time.

Supported Products

The MEGA-FIFO supports all OMEGA® data acquisition boards which have a DT-Connect interface. The list includes: CIO-DAS16-M1, CIO-DAS16-330, CIO-DAS1600-12 and CIO-DAS1600-16.

Programming

There is very little programming required to use a MEGA-FIFO in place of A/D transfers to PC memory. First, the data acquisition board must be set to transfer samples to the DT-Connect.

From high level languages, you have two choices. Employ the MEGA-FIFO support included in the Universal Driver, or you can program the MEGA-FIFO directly using the I/O registers.

Each register is two bytes in length, because the board uses the 16-bit PC-AT type bus.

Software Support

The CIO-DAS16-M1 is supplied with InstaCal software for calibration and testing. In addition, it is also supported by the optional Universal Library. The Universal Library is a set of I/O libraries and drivers for users creating their own custom programs. The Universal Library is compatible with most Windows (16-bit and 32-bit) based languages (DLL and VXD), and it supports the entire CIO family of boards. The Library includes an extensive set of programming examples written in Visual Basic and C.

An optional driver for LabVIEW is also available.

Specifications

CIO-DAS16-M1

Channels: 8 Differential

A/D Type: 12-bit subranging flash for CIO-DAS16-M1; 16-bit subranging flash for CIO-DAS16-M1-16

Input Ranges: ± 10 V, ± 5 V, ± 2.5 V, ± 1.25 V, ± 0.625 V
0 to 10 V, 0 to 5 V, 0 to 2.5 V, 0 to 1.25 V

Conversion Time: 0.8 μS

A/D Convert & Transfer Speed: 1 MHz

Accuracy: 0.01% ± 1 LSB

Integral Linearity: ± 1 LSB
No missing codes guaranteed over temp. range

Maximum Overvoltage: ± 35 V Continuous

Input Leakage Current: 250 nA max @ 25°C

Gain Drift: ± 35 ppm/°C max

Zero Drift: ± 25 ppm/°C max

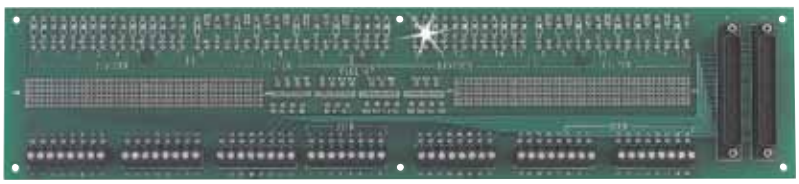
Counters: CIO-DAS16-M1 has 3 counters, dedicated to A/D timing;
CIO-DAS16-M1-16 has 9 counters, 4 available to user

MEGA-FIFO

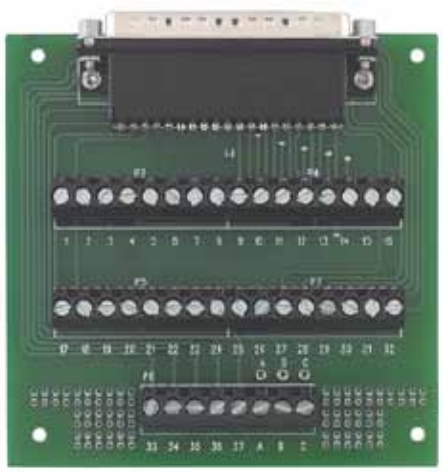
Configuration: 1 to 8 banks of user-supplied and -installed SIMM memory, 2 modules per bank

SIMM Size: 256 K, 1 MB, 4 MB or 16 MB (30 x 9)

Memory Addressing: Sequential, auto increment reset to address zero



The CIO-TERMINAL shown smaller than actual size.



The CIO-MINI37 shown smaller than actual size.

Access Time:
80 nS or faster

Memory Refresh: Synchronized to system refresh

Maximum Sample Size:
2 MS, 8 MS, 32 MS or 128 MS

DT-Connect Max Rate:
1 million samples per second, max

PC Bus Transfer Rate: 900 K samples/second type

OMEGACARE Extended Warranty Program

OMEGACARE℠ extended warranty program is available for models shown on this page. Ask your sales representative for full details when placing an order. OMEGACARE℠ covers parts, labor and equivalent loaners.

To Order

Model Number	Description
CIO-DAS16-M1	1 MHz 8-channel 12-bit analog input with programmable gain queue, 32 digital I/O and 3 counter/timers
CIO-DAS16-M1-16	1 MHz 8-channel 16-bit analog input with programmable gain queue, 32 digital I/O and 9 counter/timers
MEGA-FIFO	128 million sample buffer for CIO-DAS16-M1 series acquisition boards, or any DT-Connect equipped boards (includes cable that connects to DT-Connect boards) (does not include memory)
C37FF-2	2' 37-pin analog input cable for CIO-DAS16-M1 boards
CIO-MINI37	Screw terminal panel, 4 x 4" (102 x 102 mm) for connecting inputs to CIO-DAS16-M1 boards (requires cable)
CIO-TERMINAL	Screw terminal panel, 16 x 4" (406 x 102 mm) with prototype area (requires cable)

***CIO-DAS16** Series comes with a complete operator's manual and InstaCal software. The **MEGA-FIFO** is used to store up to 128 million samples; however, **CIO-DAS16-M1** boards can operate without the **MEGA-FIFO** if acquiring fewer samples.*

OMEGACARE℠ extended warranty is available for models shown on this page. Ask your sales representative for full details when placing order.

Ordering Example: CIO-DAS16-M1** card with one **C37FF-2** cable, one **CIO-MINI37** screw terminal panel, **OCW-1,** OMEGACARE ℠ extends standard 3-year warranty to a total of 4 years. and **MEGA-FIFO.